BLIND BURIED AND/OR FILLED VIAS

There are three frequently asked questions about blind, buried or filled vias.

- What are they?
- Why do I need them?
- Why do they cost a lot more?

There is not a simple explanation beyond the fact that they cost more. However, to understand the reason behind the extra cost and why using them is a wise choice for modern complex designs requires a definition of industry terms (Acronyms), and an explanation of what they are and how they are created by the fabrication shop.

ACRONYMS
(In the order they appear in the explanation below)

**PCB** Printed Circuit board. Usually applied to the completed product consisting a fiberglass core with copper traces’n’spaces on the outer surfaces.

**TRACE’n’SPACE** The pattern applied to the layers of a PCB. These come from the design software and are contained in the “Gerber File” to the fabricator. They are usually designated by a thickness (in mils) of the trace followed by the thickness of the isolating space between the traces. For example, 5/6 refers to a 5 mil trace and a 6 mil space.

**CORE** A thin piece of fiberglass laminate with copper cladding on both sides. Core has fully cured epoxy and is intended to be buried within a multi-layer PCB structure. It is available in a wide range of thicknesses and of copper foil weights.

**PhotoMask** A photo sensitive material applied to the copper foil of the core or the outer layers of a PCB to allow the transfer (photographically) of the computer-generated (CAD) image in the Gerber file to the copper surface of the core or outer layer of the PCB

**ETCHING** A process of removing a base layer of copper leaving only the desired Traces’n’Spaces. The etching solution is masked from the traces’n’spaces by a photomask such that only the exposed base layer of copper is etched. This process continues to the surface of the laminate until all of the traces’n’spaces are un-shorted and there is no residual copper left between the traces.

**LAYUP** The process in a multi-layer PCB where the cores are sandwiched between layers of glass matt that are saturated with an uncured epoxy. The layers provide the insulating material between copper layers of traces’n’spaces and they also provide the “glue” that bonds the inner layers together.

**PREPREG** These are thin sheets of a woven glass matt that are saturated with a “B-Stage” epoxy that is dry to the touch, but uncured. When exposed to temperatures above the melting point of the epoxy, the B-stage flows around the copper circuitry (above and below) removing any air, filling all geometry, and bonding the surfaces together as it cures.

**Prepreg** is available is a wide variety of thickness due to the size and type of glass used to weave the matt. The variety is further expanded by the types of epoxy resin saturating the matt. The resin varies depending upon the amount of flow that is desired when the epoxy is liquid.

**1 Oz Copper** The copper foil used by a fabricator is sold to them by weight. The weight is based on a uniform film of copper spread over 1 ft² of surface. If 1 ounce of copper is uniformly spread over the 1 ft², the thickness of the resulting copper is 1.4 mils (.0014”) thick.

SLB NOTE:
“A customer request for “1 ounce copper” on the surface is due to a mis-understanding of how the term is actually applied. While the fabricator does purchase the copper foil by weight (1 oz, 2 oz, etc.) this designation is incorrect once the fabrication process begins. The purchased foil is either eroded chemically (and mechanically) or increased by electroless or electro plating. Fabricators ignore this customer mis-application of the terms and instead defer to an IPC–A-600 definition of “Thickness after Processing” which re-defines ounces into a thickness of copper. (For example, 2 Oz is defined as (after processing) of being 2.2 mils instead of 2.8 mils).”

BRICK This is a fabricator term for the double side copper clad structure that comes out of a laminating press once the Core, Prepreg, and Copper foil have all been “pressed” together and the epoxy has cured. To the untrained eye, the “brick” looks like a piece of double side copper-clad laminate.

SEQUENTIAL LAMINATION Sequential Lamination refers to a repetition of the lamination process. If sequential lamination is employed, its purpose is to create an “intermediate Brick” that is intended to be used for additional processes. In sequential lamination, multiple intermediate bricks or a combination of intermediate bricks and double side cores are bonded together. This process can be repeated multiple times depending upon the process capability of the fabrication shop. The typical number of laminations is 3, but a few very specialized shops can perform 5-6. These are very rare shops.

BASIC PROCESS DESCRIPTION FOR MLB AND DSB

MULTI-LAYER PCB (MLB) PROCESS
The simplest MLB starts with a double side “Core”. This thin inner-layer material has copper on both sides. The copper surface is prepped with a photo sensitive material that can be exposed by the application of UV light. The light is applied either through a photomask or with a raster scan laser (called, Laser Direct Image). The exposed areas of the photomask are used to mask the copper traces’n’spaces from an etching process (usually cupric chloride in a spray application). The exposed copper of the core is etched away leaving the core with the trace/n/space pattern of the inner layer. This is only a “Print’n’Etch” process. There are no holes in the core at this stage. The etched inner layers are further processed chemically and then (in a layup process) sandwiched between pre-preg (glass matt that is saturated with a B-stage epoxy), placed in a heated laminating press and cured into a single piece. Thin copper sheets (typically 1 ounce or 1.4 mils thickness) are laminated with the core and pre-preg such that the resulting “Brick” resembles an unprocessed sheet of Double Side Laminate.

THE DOUBLE SIDE (DSB) PROCESS
The final process stage of all PCBs is the double side process. This is true for even the most complex multi-layer PCBs. At this stage, there is a core of fiberglass (with or without inner-layers) covered by a thin layer of copper on both sides. The double side “Brick” is then:
- Drilled
- Chemically processed (Prepare the drilled hole for adhesion of the thru-hole plating)
- Thru-hole plated (Electroless copper that is very thin)
- Photo imaged (to transfer the outer layer pattern of traces’n’spaces)
- Electro-plated (to build the final thickness of copper in the thru-holes)
- Etched (to remove the base layer of copper)
VIA EXPLANATION AND PROCESS

THRU-HOLE VIA
The via hole is the means of connecting an electrical trace to the opposite side of a PCB. It is in essence a “cylindrical” trace created by copper plating a drilled hole to a typical wall thickness of 1 mil (.001). To create the via hole, a “landing” pad is required on each side of the PCB. When viewed from a “edge on” perspective, the cross section of a plated via hole looks like a rivet with a button head on the top and the bottom. Because a landing pad is required to create the plated via, each via consumes a significant amount of area on the PCB. The smallest drilled via is going to have a landing pad of about 20 mils (.020” or .5mm) in diameter. A typical MLB will have hundreds of via holes. These create a great challenge for the designer as they attempt to rout traces’n’spaces around the inconvenient via landing pads.

BURIED VIA
A buried via is employed to greatly increase the density of the traces’n’spaces within a PCB. It allows a significant increase in the area available to the PCB designer for traces’n’spaces on the outer two layers since the buried via holes do not penetrate the outer layers. The same is true of any internal signal layers that do not contain the buried vias. The designer can make connections between traces without going “up” or “down” to an outer layer. This is a huge benefit when the traces must emulate coaxial cables and have a characteristic AC impedance. Thru-hole vias provide a significant barrier to the routing of these “controlled impedance” traces.

A buried via is created by first processing one or more double side PCBs. A very thin double side core (2 layers within a multi-layer PCB) is processed as a complete plated-through DSB. This requires different process equipment from a “standard” double side board due to the thickness of the core (a core can be a thin as a sheet of paper). Yet, all of the thru-hole processes are required with the exception of solder mask and final surface finish. These thin PTH cores are sandwiched between resin-rich pre-preg (above and below) and then pressed together to create a multilayer PCB.

At this stage, the “brick” as it is called by the industry can be processed as a double side PCB. The pre-preg must have sufficient resin (epoxy) content to not only fill the 3-D geometry created by the traces’n’spaces, but ALSO the additional geometry of the center of the plated via holes.

SEQUENTIAL LAMINATION FOR BURIED VIAS
For additional density, each layer pair in a MLB can have its own buried vias. These layer pairs are then (in the layup process) laminated into the final “Brick” for outer layer processing. However, even this structure can be further expanded by combining pairs of internal layers containing buried vias in a process called, “Sequential Lamination”. Sequential lamination creates an intermediate “brick” of 4 or more layers with each layer pair having their own buried vias. Then the intermediate brick can have thru-hole vias that join the layer pairs (an intermediate brick can be drilled and processed with its own buried vias).

Two or more intermediate bricks can then be combined to create an additional intermediate brick with even higher density. This process can be performed a maximum of 5-6 times (3 is the recommendation
due to copper thicknesses that are accumulating on the inner layers and registration issues that result from this many photo/chemical/mechanical operations)

“Buried vias are very robust and are often employed in controlled impedance designs. However, they add cost due to the need to process a complete DSB and then start the conventional MLB process. Another way of thinking of buried vias is that you are purchasing a double side PCB as well as a multi-layer PCB. With sequential lamination, you are purchasing multiple DSBs as well as a multi-layer PCB”

**BLIND VIAS**
The blind via has become popular as more fab shops have the ability to perform a controlled depth drill operation with a laser drill. The most common application of the blind via is to remove the “congestion” created by the “fan-out” of “dog bone” traces to a thru-hole via under high density BGAs. These fan out traces and their terminating thru-hole via use huge amounts of real estate, require the use of very small traces’n’spaces, and require the use of very small (and fragile) solder mask dams between the geometry. The terminating via (with a landing pad) consumes routing space for traces that need to go to other BGA pads, requiring these to happen on an inner layer. The small traces’n’spaces add cost due to the yield at the fabricator to produce these small traces’n’spaces on outer layers.
The landing via pads also create a physical barrier to the size of the BGA balls/pads that can used. There are many new high density BGAs that cannot use a copper dog bone PCB pattern with landing pads for thru-hole vias.

Further, from an assembler’s perspective, the dog bone pattern or (even worse) the solder mask defined pad process are a huge problem as they attempt to use conventional stencil print processes for the application of the solder paste to the BGA pads. The reason is that a stencil process requires that the extruded solder paste be able to adhere to the PCB pad such that it is removed (pulled) as a “pattern” from the aperture of the metal stencil when the stencil “snaps” away from the PCB surface. The stencil process needs a solid “gasket” to the corresponding pad to be pasted. If the stencil is not able to gasket to the pad, then the amount (volume) of paste that is deposited is significantly reduced. Any non-uniformity in the height of the surface of the PCB exacerbates this stencil gasketing problem. If the dog bone patterns and the copper floods for solder mask defined pads are viewed “end on”, they are at the same height as the BGA pads. However, once the solder mask is applied, then the (very) non-uniform thickness of the solder mask over the copper floods and the dog bone traces/via landing pads creates a 3-D topography for the stencil. The stencil contacts the solder mask first and then must slightly deform (about 1 mil) to make contact with the BGA pads that are lower than the solder mask. This irregular geometry results in a significant variation in the deposition of the solder paste on a given BGA pad. The advent of very good solder paste inspection (SPI) equipment has reduced the defects experienced by the assembler since the systems reject PCBs that have insufficient paste. However, the same systems are creating a significant bottleneck as PCBs with insufficient paste deposition are rejected and must be cleaned and re-stenciled.

There are numerous processes for creating the blind via. The oldest is perhaps the easiest to comprehend. In this case, the multi-layer Brick is photo masked and etched to reveal “windows” in the copper foil. These windows are then laser drilled (CO\(_2\) laser) to a controlled depth that is typically 4 mil (.004” or 0.1mm). The reason for the etching process (to create the windows) is to allow a pattern that will deflect the beam of the CO2 laser everywhere but the area under the opening which is to be ablated
to the copper pad on the next layer. Following the laser ablation of the fiberglass covering the inner layer pad, the brick is mechanically drilled for the thru-hole vias and then processed as a DSB with the conventional thru-hole plating.

The thru-holes are plated in a normal fashion (see the above DSB process), resulting in a copper “cup” that is formed in the BGA pad that makes an attachment to the corresponding copper pad on the next inner layer. This copper attachment to an inner layer allows a “pads only” outer surface for the attachment of the BGA.

However, the process described will leave a “dimple” of approximately 3 mils in depth and 4 mils in diameter in the BGA pad. For larger BGAs, this is not an issue. However as the diameter of the BGA pad approaches .2mm (10 mils), the dimple consumes a significant volume of the applied solder paste.

Different (and modern) process are employed with additional process steps, that include terms like Reverse Pulse Plating (RPP), are used to solve this problem to copper fill the “dimple” or copper cap the dimple if a resin fill of the thru-hole vias is employed. Therefore, while blind vias replicate the thru-hole plating process, they are created with different and more expensive equipment for each process operation.

“Blind vias with modern technology require multiple additional process steps with very expensive capital equipment (Laser Drill, RPP equipment, Laser Direct Image, etc.). For these reasons, Blind vias can be thought of as doubling the process required to produce the traces’n’spaces and plated holes for the outer layers.”

Blind vias and buried vias are not mutually exclusive, and a design can employ either or both. Today’s high density PCBs frequently require at least the use of blind vias to increase the yield at the fabricator and the assembler. While they do increase the cost of the PCB, the reliability and process consistency will offset the additional PCB cost. It is a false sense of economy to accept the process variation and structural degradation that conventional processes will create when a .25mm BGA is utilized.

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Two or more intermediate bricks can then be combined to create an additional intermediate brick with even higher density. This process can be performed a maximum of 5 times (3 is the recommendation) due to copper thickness that are accumulating on the inner layers and registration issues that result from this many photo/chemical/mechanical operations.

**VIA-IN-PAD w/RESIN FILL AND COPPER CAP**

A lower cost alternative to the blind vias is a process that fills the thru-hole vias and vias in the BGA pads with a resin that replicates the coefficient of thermal expansion of the epoxy used in the pre-preg. This process is very viable when the trace’n’space density does not require blind vias, but high density BGAs are being employed.

In this process, the thru-hole vias and vias in the BGA pads are drilled and then thru-hole plated. This is followed by a panel electro-plate to increase the copper thickness in the via holes and vias in the BGA pads (the thru-holes for components must be done in a second
drilling and plating step). The plated via and BGA holes (no pattern has been applied) are then pressure-plugged with an epoxy resin that is Tg matched to the pre-preg. The resin is cured and then mechanically planarized to match the surface of the outer layer copper foil. The panel with resin-filled via holes is processed through the complete DSB process (drilling, plating, etching, etc.) for the component holes that must be left open for thru-hole pins. This process puts a copper cap over the resin dots in the via holes and the BGA pads! The end result is a BGA pads only outer layer that is easily stencil printed with solder paste.

STACKED VIAS
Stacked vias are used in very (extremely) high density designs where the real estate to fan out to buried vias is not available. In this case, a blind via is “stacked” over a blind via on an “intermediate Brick” instead of a copper inner layer pad. This process requires sequential lamination, but it also requires that the blind via process be performed on the intermediate brick before the next lamination process.

Stacked vias are not for the faint of heart. They can be made reliable but to do so requires a close cooperation between the designer and the fab shop. This technology cannot be designed in a vacuum and then sent out for bid. The most common failure is a Coefficient of Thermal Expansion (CTE) mis-match of all of the resins in the MLB. During subsequent processing by the assembler, the CTE of each resin (pre-preg, core, resin fill) will expand at a different rate. In all thermo plastics, the CTE goes from approximately linear to exponential once the Glass Transition Temperature (Tg) of the different resins have been exceeded. If the fabricator simply matches data sheets without performing flow tests on each type of resin he has created a prescription for disaster for the assembler. Any CTE mismatches will result in a fracture of the stacked via during the SMT fusion or even the through-hole soldering process. All MLB resins melt below the fusion temperatures of lead-free solder……

“I sincerely hope this explanation clears some of the questions about when and why to use different via structures. I am saddened with the responses attributed to our industry as they seem to gloss over these distinctions. I find most customers have been callously confused by the concatenation of acronyms (gobble gook) by our industry’s purveyors of knowledge.”

Respectfully,

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